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IMPROVEMENT OF POWER QUALITY USING FUZZY LOGIC CONTROLLER BASED CASCADED MULTI-LEVEL CONVERTER INTERCONNECTED TO GRID

(Chittem Hema[1] Dr.E.Kiran Kumar[2])

[1](M.Tech Student, Dept. of Electrical and Electronics Engineering, Swetha Institute of Technology and Science, India)

Email Id: hemac9989@gmail.com

[2](Professor, Dept. of Electrical and Electronics Engineering, Swetha Institute of Technology and Science, India)
Email Id: endala.kirankumar@gmail.com

Abstract:

This paper looks at the use of a fell staggered converter for versatile power shaping in sharp lattice applications. The essential part of the proposed scheme is the usage of free DC joins, with diminished voltages, which makes such a geology an ideal opportunities for medium and high power applications with extended unfaltering quality. The made control framework oversees independent DC-interface voltages in each H-associate cell and grants specific and versatile compensation of disturbing streams under a grouping of voltage conditions without requiring any reference layout change. The specific control philosophies rely upon the disintegrations proposed in the Conservative Power Theory (CPT), which achieve a couple of current-related terms related with unequivocal weight credits. These current portions are independent of each other and may be used to portray unmistakable compensation frameworks, which can be explicit in restricting explicit effects of disturbing weights. Diversion results are given to affirm the possible results and execution of the proposed control frameworks, considering ideal and disintegrated voltage conditions are made in MATLAB/SIMULINK

Index Terms: Active power filters, Compensation strategies, multilevel inverter, Reactive compensation, Selective compensation, and Unbalance compensation.

I.INTRODUCTION

Electronic frameworks and a few nonlinear burdens have been progressively utilized since the appearance of intensity hardware. Such gadgets are generally progressively effective and adaptable in a wide scope of utilizations, for example, AC and DC engine drives, battery chargers, control supplies, uninterruptible power supplies (UPS), rectifiers, etc. In any case, the present quality weakening because of consonant contamination from exchanging gadgets has been infiltrating the utility network and causing incredible worries for the service organizations, administrators, or even normal buyers in the nearby framework. A few power molding topologies have been utilized for consonant, responsive and unequal current pay [1]-[4] and their control methodologies [5]-[9]. Concerning decision of remuneration systems to be applied, an extraordinary number of potential outcomes have been tended to, featuring the significant commitments dependent on the prompt power (PQ) hypothesis [10], [11] and synchronous reference outline (DQ) control strategy [12], [13]. In any case, there are elective systems that may demonstrate more adaptable than the ones above, giving a less difficult approach to make up for unsettling influences specifically, and disentangling our perception of the connected electrical traits. In this one of a kind circumstance, this paper proposes to use CPT [14]-[15] as an elective framework for the progression of electronic force processors (EPP), especially to the arrangement of actual segments and to the significance of explicit compensation systems for multifunctional grid tied inverters or shunt dynamic channels. This is on the grounds that the best possible decision of which bits ought to be remunerated is a basic factor for the undertaking, since the real ostensible worth straightforwardly

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impacts the prerequisites of the dynamic and latent components of the EPP, and in this manner, the monetary expense of their establishments. From the converter's topology perspective, staggered inverters have a few merits over regular inverters, for example, low all out sounds mutilation (THD), low exchanging misfortunes, great influence quality, decreased electromagnetic impedance (EMI), seclusion and low switch voltage worry of electronic parts. Among various topologies of staggered converters, for example, the unbiased point-clipped or diode-braced and the flying capacitor, fell staggered converter is one of the most prevalent. It is made out of numerous H-connect control cells. By and by, the quantity of intensity cells in a fell H-connect inverter is for the most part controlled by its working voltage and assembling cost. Fell H-connect Multilevel Inverter (CHMI) requires minimal number of segments for a similar voltage level when contrasted with different sorts of staggered inverters . The CHMI comprises of individual H-connect cells, which are bolstered by individual DC source. Every H-connect cell creates three diverse voltage levels at the yield. The arrangement association of the H-connect cells creates yield voltage waveforms that are incorporated by the mix of each yield of the H spans at certain exchanging states. For Shunt Active Power Filter (SAPF) and STATCOM applications, capacitors may be utilized at the CHMI DC-joins, rather than DC sources, and an assortment of procedures for controlling the CHMI DC-connect voltage is accounted for in the writing.

This paper proposes the control of a 7-level SAPF CHMI with individual H-connect DC-interface voltage guideline, applied for specific pay or minimization of specific burden unsettling influences, under an assortment of voltage conditions. The displayed control technique is secluded, and it very well may be adjusted to any number of modules in arrangement. CPT is utilized as an option for producing an assortment of current references in the stationary casing, for specific unsettling influences relief and if necessary, dynamic power infusion. Contrasted with the underlying proposition in, new discoveries and exploratory outcomes were incorporated to help the hypothetical examination.

II. CHMI STRUCTURE AND MODULATION

The CHMI is made out of a progression of fell H-connects, each encouraged by free DC sources [19]. Every H-connect as a power cell is prepared for three particular voltage levels at the yield. The course of action relationship of the H-ranges produces yields voltage waveforms that are mixed by the blend of each yield of the H-ranges at certain trading states. This geography offers various great conditions, for instance, the component of estimated quality, control and protection necessities of each framework cell. The fell staggered shunt converter is demonstrated in Fig. 1, where it is additionally conceivable to see the system burdens associated at the purpose of normal coupling (PCC). The PCC burdens are comprised by both adjusted and uneven direct and nonlinear gadgets. The yield voltage waveform in each stage is gotten by including the H-connect cells yield voltages as pursues:

$$v_o(t) = v_{o,1}(t) + v_{o,2}(t) + \cdots + v_{o,N}(t) = \sum_{k=1}^{N} v_{o,k}(t), \quad (1)$$

Where N is the quantity of H-connect cells.

In the event that all DC-voltage sources in Fig.1 are equivalent to Vdc, the inverter is then known as a symmetric CHMI. The quantity of yield levels (N_L) in a symmetric CHMI is identified with the quantity of H-spans (N) by the accompanying condition:

$$N_L = 1 + 2N. \quad (2)$$

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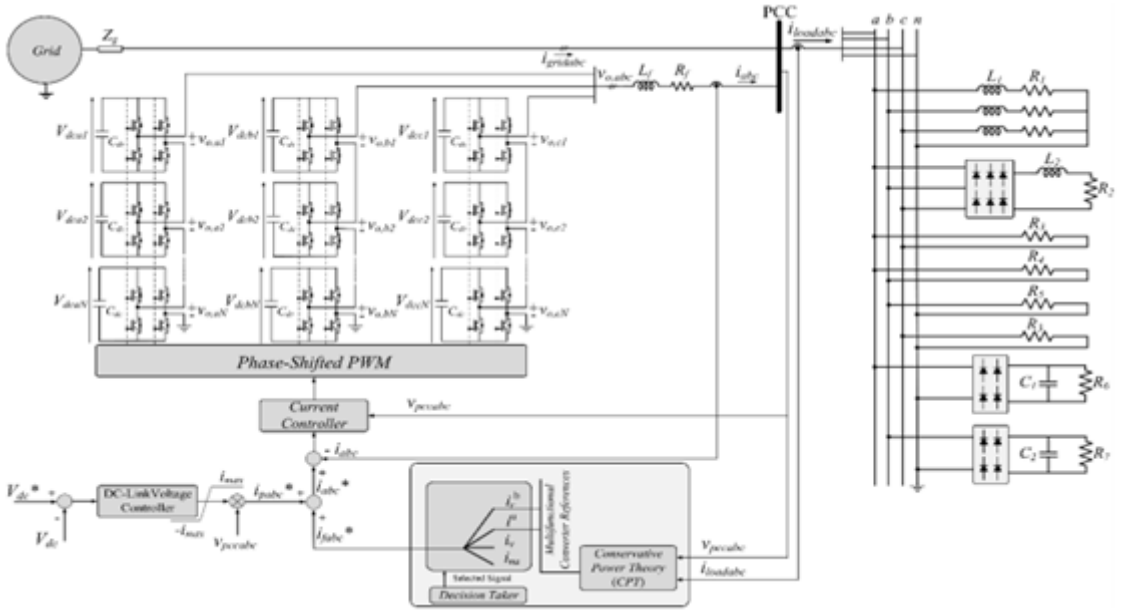

Fig.1.Block diagram of the power circuit, control scheme, and loads to the power grid.

The maximum output voltage, is then obtained as:

$$V_{o,MAX} = NV_{dc}. \qquad (3)$$

Inconsistent sizes of the DC voltage sources in Fig.1 would bring about a deviated CHMI with an expanded number of yield levels created by a similar number of H connect cells. Adjustment systems for CHMI are an expansion of the customary two-level exchanging plans. Different regulation procedures have been displayed for CHMI to switch the transistors in every cell. By their exchanging recurrence, they can be for the most part grouped either as crucial or high exchanging frequencies. The principal approach recommends lower exchanging misfortunes, however the music in the yield voltage waveform show up at lower frequencies. Low-recurrence procedures, for example, Selective Harmonic Elimination (SHE) and Space Vector Control (SVC) are applied to high power and low unique frameworks. For the subsequent methodology, the music are products of the exchanging recurrence and their sidebands. Space Vector Modulation (SVM) and Carrier based PWM are instances of high-recurrence methodologies. The Carrier-based adjustment plans can be separated into two classifications: Phase-Shifted (PS-PWM) and Level-Shifted (LS-PWM) techniques. In this paper, Phase-Shifted PWM (PS-PWM) is utilized to switch the fell H-connect cells. Since every H-connect cell is a three-level converter, the customary unipolar PWM exchanging plans are received. The arrangement associated H connect cells of the converter are tweaked with individual transporter waveforms while having a similar reference signals. A stage move among the bearer waveforms is applied to nearby H-connect cells. The point of the stage move relies upon the degree of the converter and is customized to the particular exchanging plan, which is actualized in every H-connect cell. Ideal symphonious scratch-off can be accomplished when the stage move between the bearers is 180°/, where N is the quantity of arrangement associated H-connect cells. In this paper, the CHMI is made out of three modules, incorporating a 7-level yield voltage waveform. The triangular transporters with a stage move of 60° are contrasted and two sinusoidal references for the exhibited 7-level CHMI is outlined in Fig. 2.

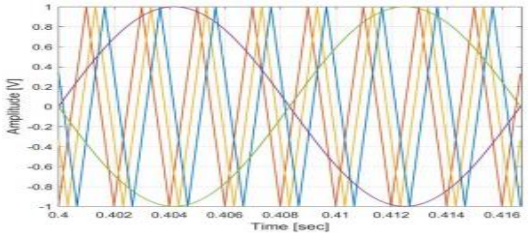

Fig.2.Reference and carrier signals for one phase of the 7-level CHMI.

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The implementation of a 60° Phase shift among the three PWM triangular carriers inside the simulation block for the 7-level CHMI is shown in Fig. 3.

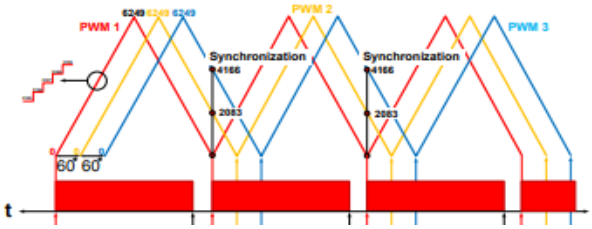

Fig.3. Implementation of the PS-PWM for the 7-level CHMI.

III. CURRENT AND POWER DECOMPOSITIONS IN A MULTIPHASE CIRCUIT USING CPT

The CPT [14] takes into account the deterioration of the prompt flows into various symmetrical current terms, substantial for single-and multiphase frameworks, freely of the voltage conditions. Such parts can be applied as reference sign to shunt dynamic channels [15], multifunctional converters , or for the plan of channel components, for example, semiconductor switches, inductors, and capacitors. Additionally, the subsequent pay systems are profoundly adaptable, since the deteriorations take into consideration the particular distinguishing proof and minimization of various troublesome impacts (nonlinearities, unbalances, responsive power). In this way, accepting a multiphase circuit where each period of the framework is meant by the subscript m, one may have:

- adjusted dynamic flows i^b_{am} amwhich are identified with the dynamic power utilization;
- adjusted responsive flows i^b_{am}_am, which are identified with the receptive power dissemination;
- void flows i_{vm} which are identified with the nonlinear (mutilation) conduct among voltages and burden flows;
- unbalanced currents(i^u_m, $= i^u_{am} + i^u_{rm}$) which are related to the unbalanced load behavior;
- Non-active currents (i_{nam}), which represents all the unwanted terms of the load currents ($i_{nam} = i^b_{am} + i_{vm} + i^u_m$).

By definition, the collective RMS current can be split into:

$$I^2 = I_a^{b2} + I_{na}{}^2 = I_a^{b2} + I_r^{b2} + I^{u2} + I_v{}^2, \quad (5)$$

Indicating that all current components are orthogonal to each other and they could be controlled or minimized selectively. Thus, the apparent power may be calculated as:

$$A^2 = V^2 \cdot I^2 = P^2 + Q^2 + N^2 + D^2, \quad (6)$$

Where:

$P = V \cdot i^b{}_a$ is the active power (7.a)

$Q = V \cdot i^r{}_b$ is the reactive power (7.b)

$N = V \cdot i^u$ is the unbalance power (7.c)

$D = V \cdot i_v$is the void power (7.d)

From CPT, the global power factor is defined in (8), and it can be calculated in any generic circuit, independently of waveform distortions or asymmetries, representing the global efficiency of the load.

$$\lambda = \frac{P}{A} = \frac{P}{\sqrt{P^2 + Q^2 + N^2 + D^2}}. \quad (8)$$

IV. CONTROL STRATEGY

The proposed 7-level CHMI is controlled to manage the DC-connect voltages of every H-connect cell, and to repay current burden terms identified with upsetting impacts. The voltage regulator yield, from H-connect cells, is increased by the PCC voltage (v_{pccabc}), to characterize an extra current reference (i^*_{pabc}) to be added to the reference of the unsettling influence currents (i^*_{pabc}) . The coming about current reference ⟦(i^*_{abc}) is coordinated to the current regulator yield of the dynamic channel. Hence, the dynamic channel should go about as a powerful factor controlled rectifier during transient burden conditions and as a current compensator under consistent state conditions. Notice that there is no requirement for an organize change or synchronization calculation to give the reference signals. Expecting one stage (a) of the CHMI, the control procedure for DC voltage regulators of every

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H-connect cell is outlined in the chart of Fig. 4, which is involved internal and outside control circles. The internal circle coordinates the inverter yield current at the ideal reference(i^*_a) , and the outside circle controls the DC-interface voltages in each H-associate cell. The ideal inverter current is the entire of the DC interface voltage rule flows (i^*_{pa}) and the remuneration references from the CPT deterioration (i^*_{fa}).

The currently proposed controller is designed in the *abc* frame based on frequency response requirements. Consider the CHMI of Fig. 1.

A. Current controller derivation

The dynamics of the AC-side current ia is described by (9). It represents a system in which ia is the state variable, vo, are the control inputs, and $vpcca$ is the disturbance input.

$$L_f \frac{di_a(t)}{dt} + R_f i_a(t) = \sum_{k=1}^{N} v_{o,ak}(t) - v_{pcca}(t) \quad (9)$$

The H-bridge converter terminal voltages can be written as:

$$\begin{bmatrix} v_{o,a1}(t) \\ v_{o,a2,}(t) \\ \vdots \\ v_{o,aN}(t) \end{bmatrix} = \begin{bmatrix} m_{o,a1}(t)V_{dc} \\ m_{o,a2}(t)V_{dc} \\ \vdots \\ m_{o,aN}(t)V_{dc} \end{bmatrix} \quad (10)$$

Where $mo,1(t)$, $mo,a2(t)$, ..., $mo,aN(t)$ denote the modulation signals for each H-bridge converter. Their signals are continuous and their values are in the range [-1 1]. In order to facilitate the controller design and to reduce the model expressions, it is convenient to transform (10) by the definition given in (11).

$$m_{o,a}(t) = m_{o,a1}(t) = m_{o,a2}(t) = \cdots = m_{o,aN}(t) \quad (11)$$

Therefore, (9) can be rewritten as (12).

$$L_f \frac{di_a(t)}{dt} + R_f i_a(t) = NV_{dc}\, m_{o,a}(t) - v_{pcca}(t). \quad (12)$$

Assuming the CHMI of Fig. 1:

$$v_{o,a}(t) = G_{inv}\, m_{o,a}(t) = NV_{dc}\, m_{o,a}(t). \quad (13)$$

Therefore, the dynamics of the AC-side current ia is determined as (14). Based on (13), the control input $vo,_,$ can be controlled by the modulating signal mo,a.

$$L_f \frac{di_a(t)}{dt} + R_f i_a(t) = v_{o,a}(t) - v_{pcca}(t). \quad (14)$$

The last term in (14), (t), will be compensated by the feed forward action. The voltage feed-forward compensation is employed to mitigate the dynamic couplings between the CHMI and the AC system, enhancing the disturbance rejection capability of the converter system.

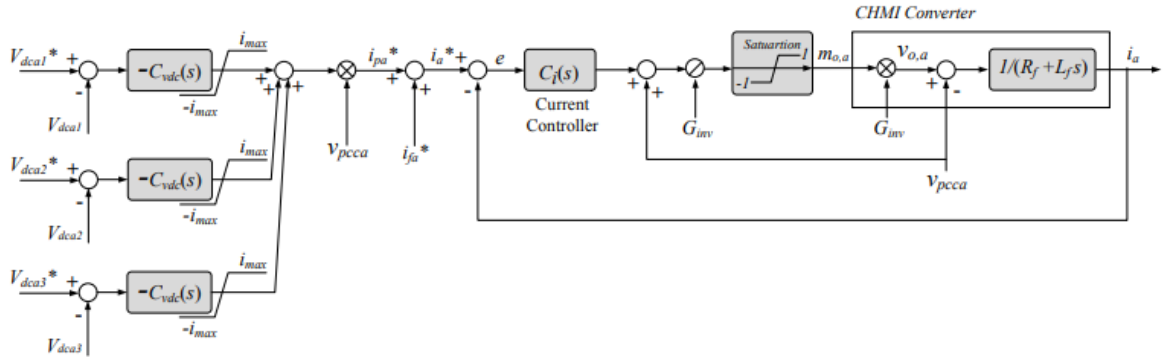

Fig.4. Block diagram of the proposed control scheme with DC voltage controllers of H-bridge cells in phase *a*.

B. DC-link controller derivation

The dimensioning of the DC-link voltage controller is based on the transfer function between the defined current reference value and the DC-link voltage in each H-bridge cell [40]. Thus, considering phase *a*, from the power balance of the inverter in this phase one may have:

$$P_{cap} + P_{ac} = 0 \quad (15)$$

$$3V_{dc}I_{cap} + \frac{V_a I_a}{2} = 0 \quad (16)$$

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Where factor 3 represents the number of H-bridge cells in phase a, Vdc is the regulated DC-link voltage for each H bridge cell, $Icap$ is the respective capacitor current, Va and Ia represent the peak value of the AC-side voltage and current of phase a respectively, and factor 1/2 comes from the average ac power flow using peak values. From (16) the current through each H-bridge cell capacitor is:

$$I_{cap} = -(\frac{V_a I_a}{6V_{dc}}) \quad \textbf{(17)}$$

And the same current regarding voltage across the capacitor is given by:

$$C_{dc}\frac{dV_{dc}}{dt} = I_{cap} \quad \textbf{(18)}$$

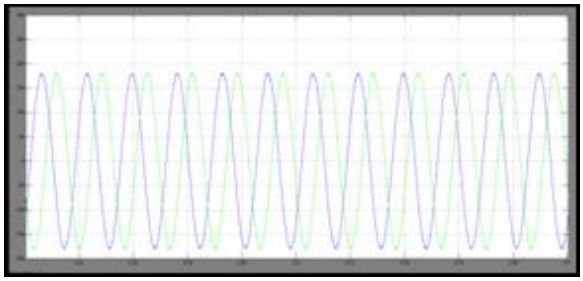
From (17) and (18) the differential equation for the DC voltage becomes:

$$\frac{dV_{dc}}{dt} = \frac{1}{C_{dc}}(\frac{-V_a\, I_a}{6V_{dc}}) \quad \textbf{(19)}$$

Based on (19), the DC-link voltage for one H-bridge cell is regulated by controlling the inverter current reference (i^*_a),. The selected bandwidth of the DC voltage loop is reduced to avoid interaction with the current controller. This means the individual capacitor voltage controllers are decoupled from the current controller as their dynamics arebacked off. In this manner, the shut current circle can be accepted perfect for structuring purposes and supplanted by solidarity. The exchange elements of the DC voltage control plot, (s), is displayed in (20). The DC-connect voltage controller (s) is duplicated by -1 to make up for the negative indication of DC transport voltage elements.

$$G_{vdc}(s) = \frac{{V_a}^2}{6V_{dc}}\frac{1}{C_{dc}s}. \quad \textbf{(20)}$$

V. SIMULATION RESULTS



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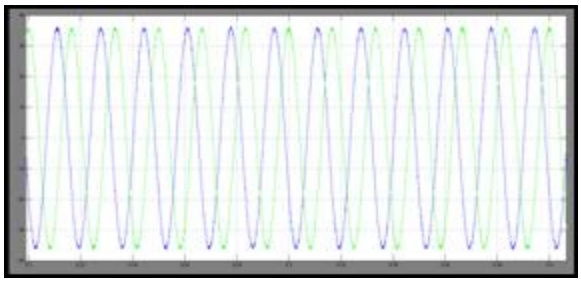
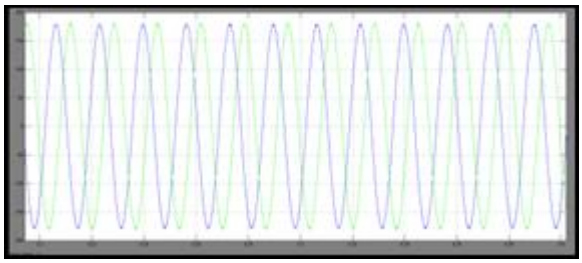


[b]

Fig: 5Before implementing any compensation strategy: (a) PCC voltage, (b) grid current



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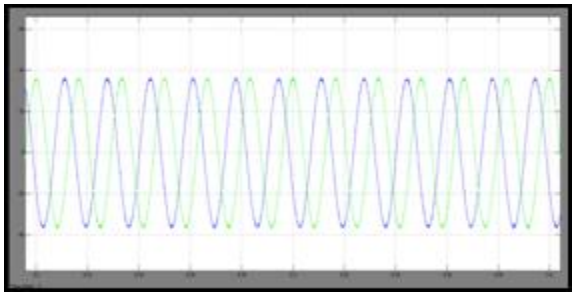

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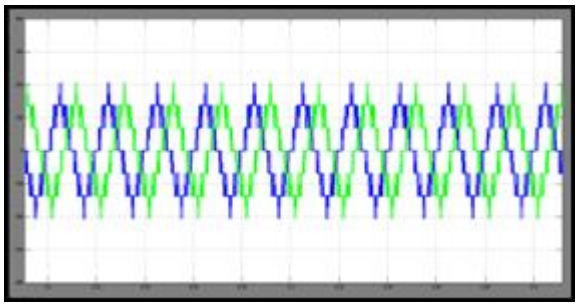

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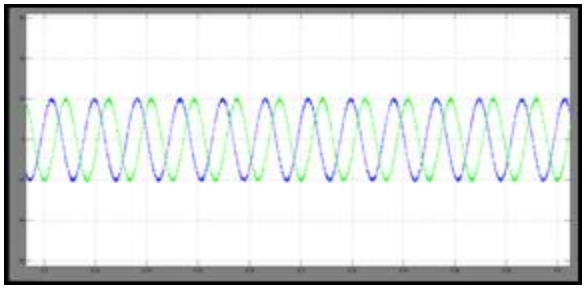

[d]

Fig: 6a Reactive Current Compensation
(a) PCC voltage, (b) grid current, (c) CHMI voltage, (d) Inverter current

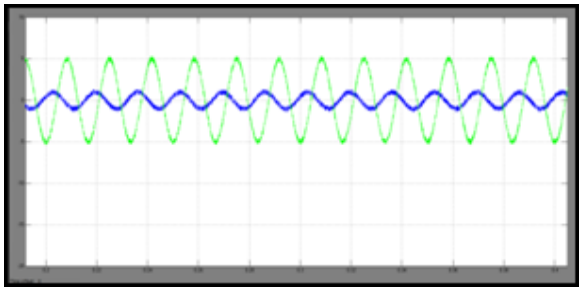

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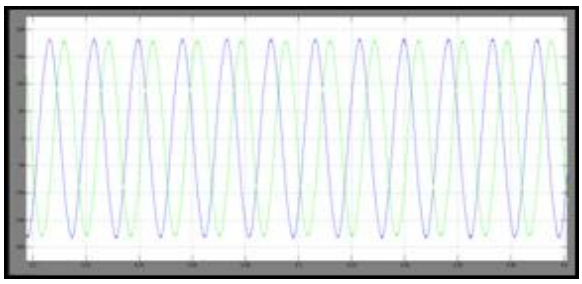
Fig: 6bUnbalanced Current Compensation
(a) PCC voltage, (b) grid current, (c) CHMI voltage, (d) Inverter current



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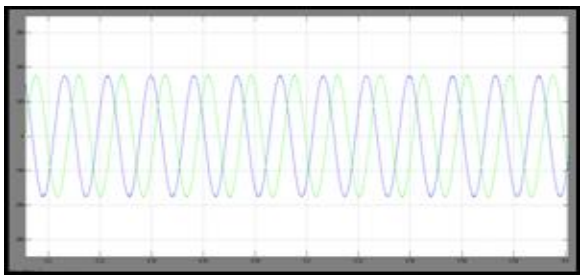

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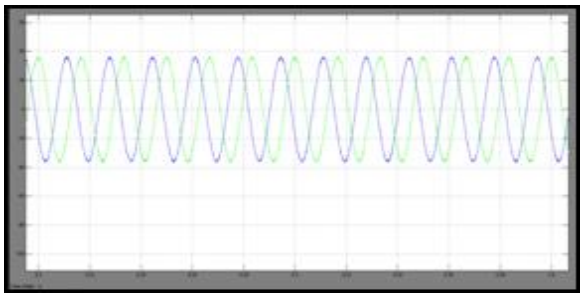

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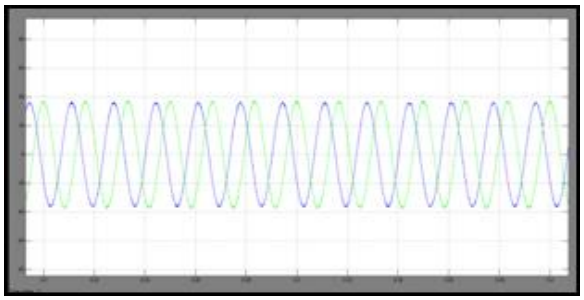

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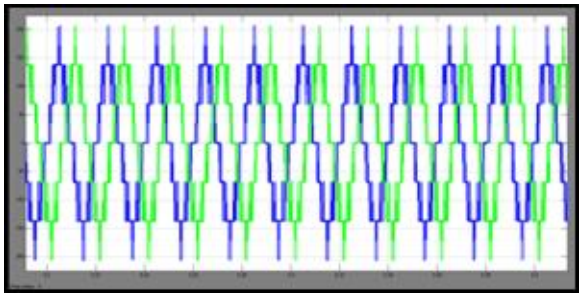

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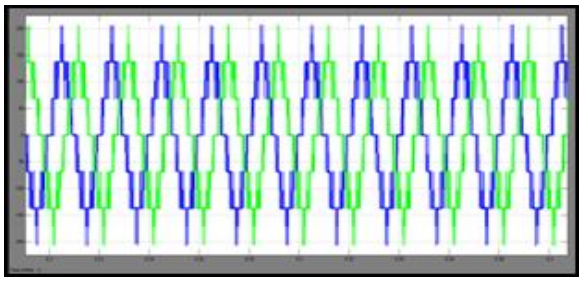

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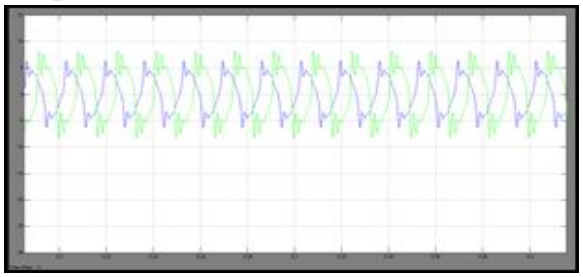

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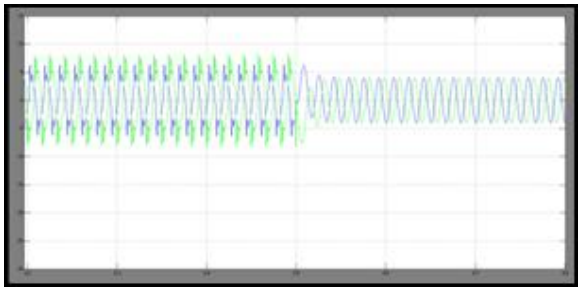

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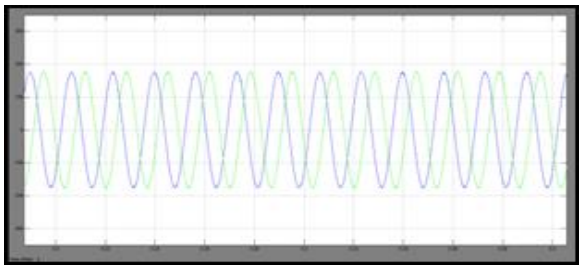
Fig: 6c Harmonic Current Compensation (a) PCC voltage, (b) grid current, (c) CHMI voltage, (d) Inverter current



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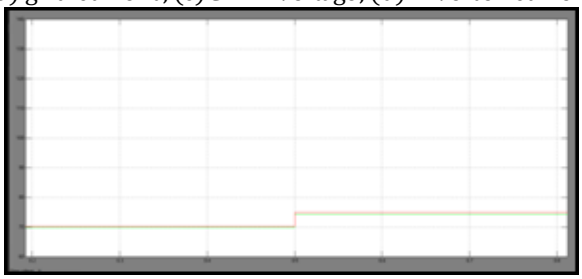

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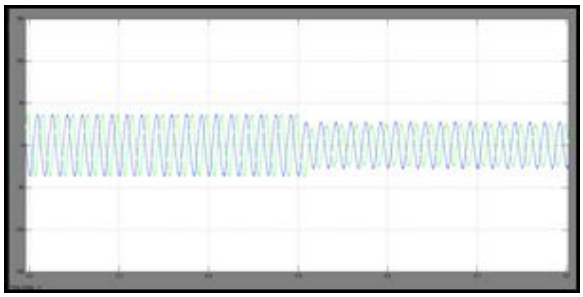

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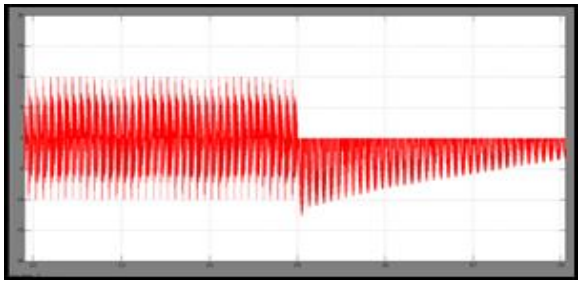
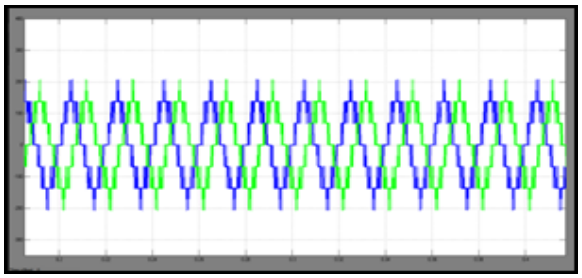


[f]

Fig: 7Dynamic response of the SAPF CHMI to sudden changes in the load: (a) PCC voltage, (b) grid current, (c) CHMI voltage, (d) Inverter current, (e) dc link voltage, (f)dc link current



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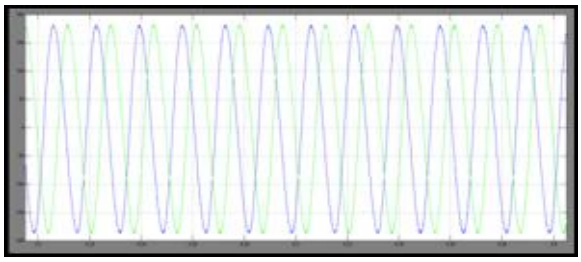

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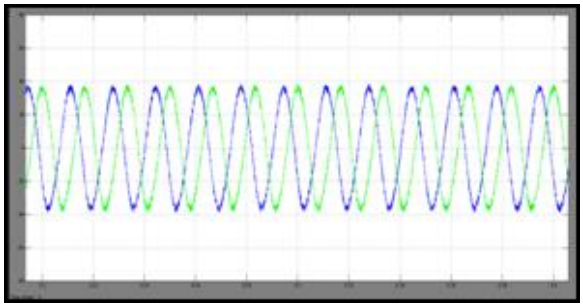

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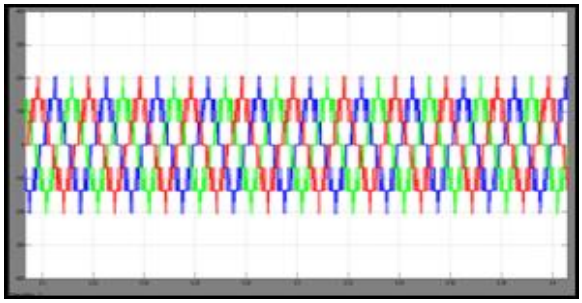

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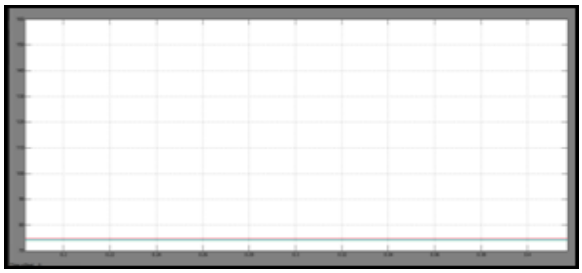

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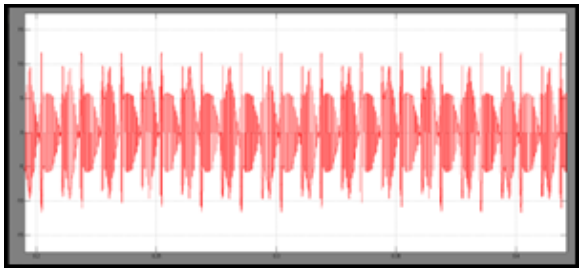
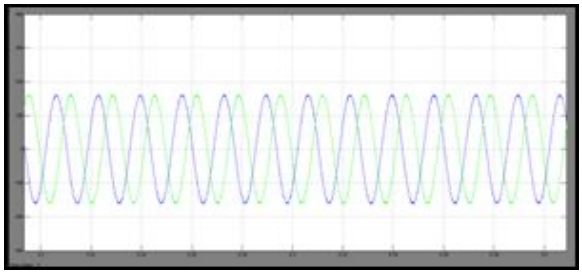


[e]

Fig: 8 Non – active Current Compensation: (a)PCC voltage, (b)grid current, (c)CHMI voltage, (d)dc link voltage, (e)dc link current



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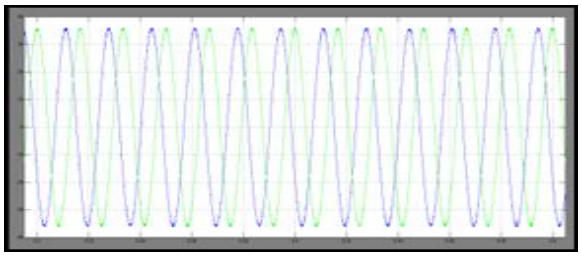
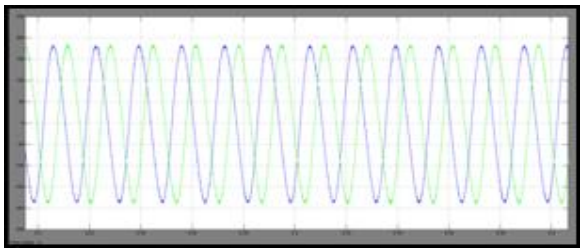


[b]

Fig: 9 Compensation of i_{na} current under asymmetrical and sinusoidal voltage source [a]PCC voltage, [b]grid current



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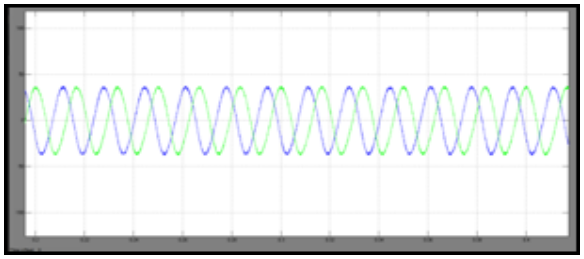

[b]

Fig: 10Compensation of i_{na} current under symmetrical and non – sinusoidal voltage source: [a]PCC voltage, [b]grid current

FUZZY LOGIC CONTROLLER

The Fuzzy Logic Controller (FLC) is utilized as controller in the proposed model. The Fuzzy Logic device was displayed in 1965, moreover by Lotfi Zadeh, and is a logical instrument for overseeing

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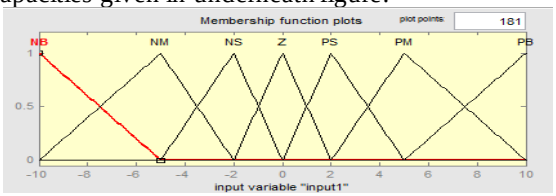
helplessness. It offers to a sensitive figuring affiliation _the critical thought of preparing with words. It outfits a strategy to oversee imprecision and information granularity. The soft speculation gives a part to addressing phonetic forms, for instance, a few, low, medium, much of the time, few. All in all, the fluffy rationale gives a derivation structure that empowers suitable human thinking abilities. In feathery justification, fundamental control is directed by a great deal of semantic rules which are constrained by the structure. Since numerical components are changed over into semantic elements, logical showing of the system isn't required. The fluffy rationale control is being proposed for controlling the inverter activity. FLC is another expansion to control hypothesis and it consolidates a straightforward, rule based IF X AND Y THEN Z way to deal with a taking care of control issue as opposed to endeavoring to display a framework scientifically.

A. Error Calculation:

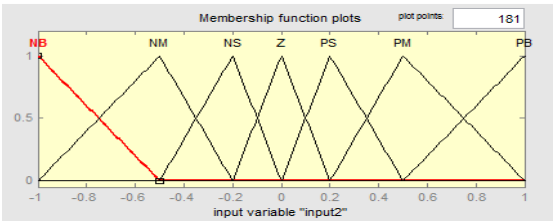
The blunder is determined from the distinction between stockpile signal information and the reference signal information. The blunder rate is the pace of progress of mistake.

B. Fuzzification:

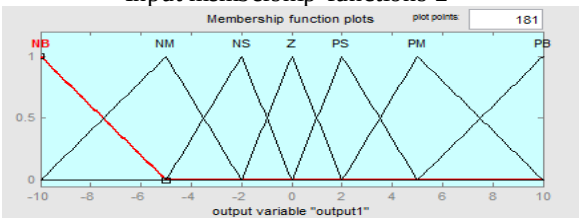
Fuzzification is a significant idea in the fluffy rationale hypothesis. Fuzzification is where the fresh amounts are changed over to fluffy. Along these lines Fuzzification procedure may include allocating participation esteems for the given fresh amounts. This unit changes the non-fluffy (numeric) input variable estimations into the fluffy set (etymological) variable that is an obviously characterized limit, without a fresh (answer). In this recreation study, the mistake and blunder rate are characterized by phonetic factors, for example, negative enormous (NB), negative medium (NM), negative little (NM), zero (Z), positive little (PS), positive medium (PM) and positive huge (PB) described by enrollment capacities given in underneath figure.



Input membership functions 1



Input membership functions 2



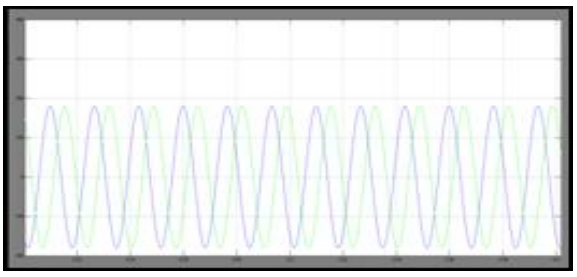
Output membership functions

C. Decision Making:

Fuzzy procedure is acknowledged by Mamdani technique. Mamdani derivation technique has been utilized in light of the fact that it can without much of a stretch get the connection between its data sources and yield. There are 49 standards for fluffy controller. The yield participation work for each standard is given by the Min (least) administrator. The Max administrator is utilized to get the joined fluffy yield from the arrangement of yields of Min administrator .The yield is delivered by the fluffy sets and fluffy rationale activities by assessing every one of the principles. A straightforward on the off chance that standard is characterized as pursues: If blunder is Z and mistake rate is Z at that point yield is Z.

IN/OP	NB	NM	NS	Z	PS	PM	PB
NB	NB	NB	NB	NM	NM	NS	Z
NM	NB	NB	NM	NM	NS	Z	PS
NS	NB	NM	NM	NS	Z	PS	PM
Z	NM	NM	NS	Z	PS	PM	PM
PS	NM	NS	Z	PS	PM	PM	PB
PM	NS	Z	PS	PM	PM	PB	PB
PB	Z	PS	PM	PM	PB	PB	PB

TABLE:1 FUZZY RULES



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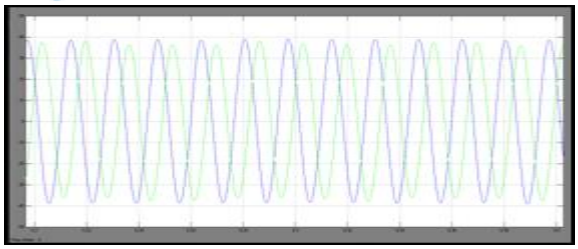
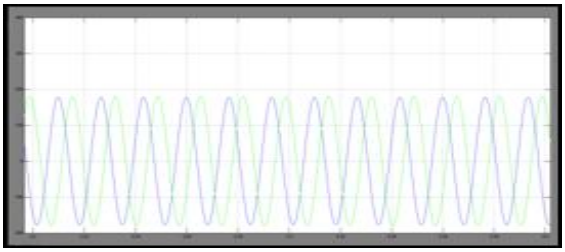


[b]

Fig: 11 fuzzy based Before implementing any compensation strategy: (a) PCC voltage, (b) grid current



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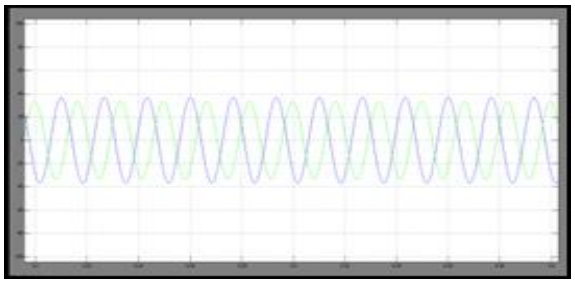

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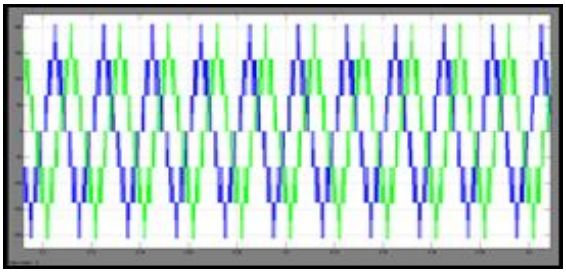

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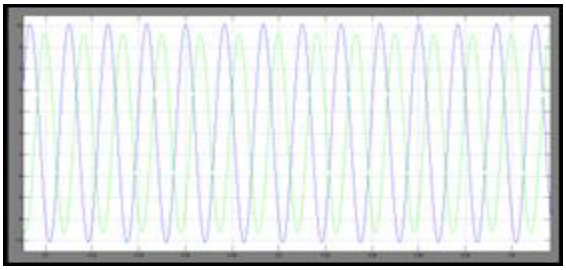
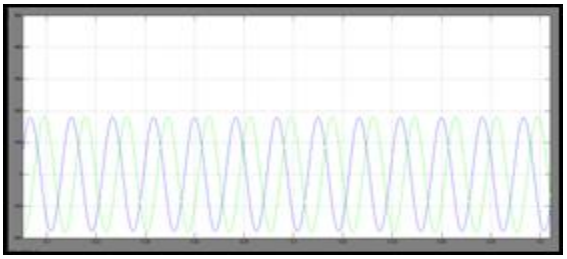


[d]

Fig: 12a fuzzy based Reactive Current Compensation (a) PCC voltage, (b)grid current, (c)CHMI voltage, (d) Inverter current



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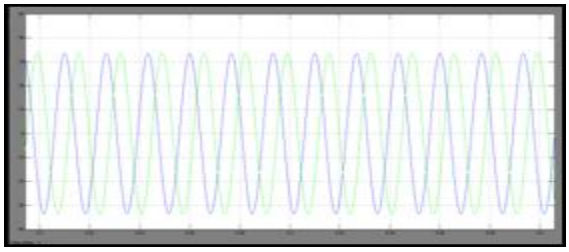

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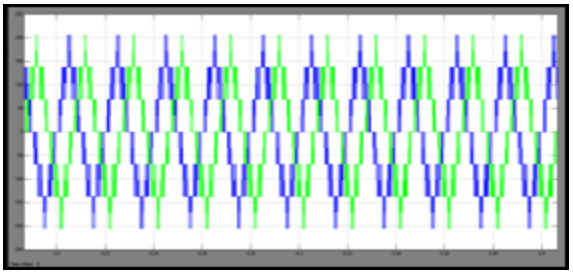

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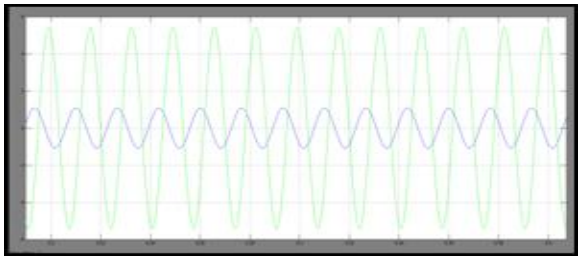

[d]

Fig: 12b fuzzy based unbalanced current compensation (a) PCC voltage, (b)grid current, (c)CHMI voltage, (d) Inverter current

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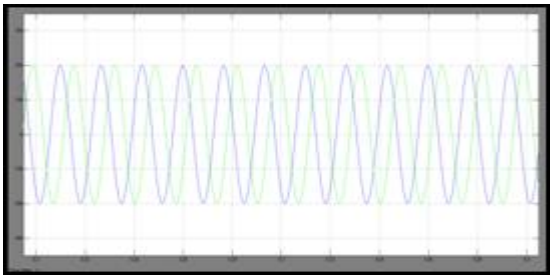

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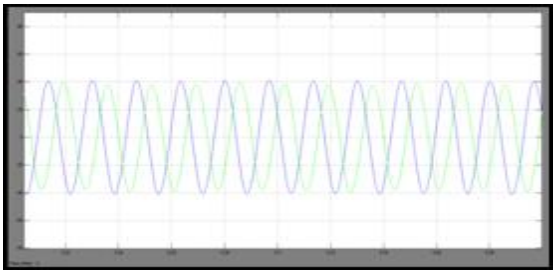

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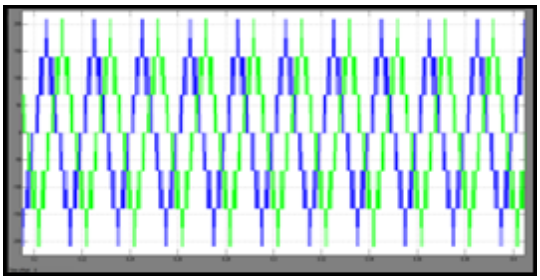

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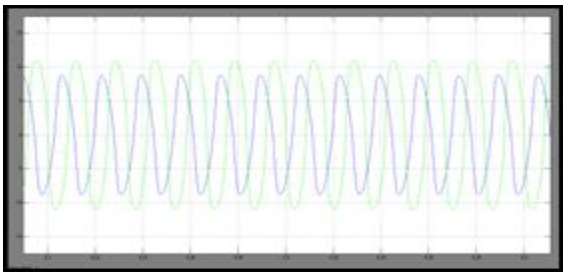
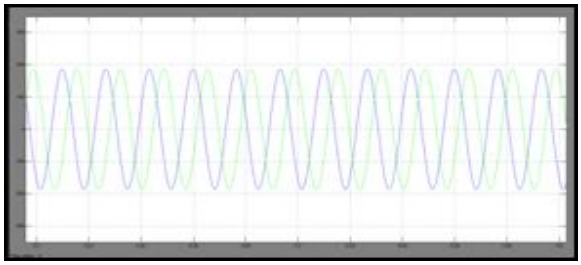


[d]

Fig: 12c fuzzy based Harmonic Current Compensation (a) PCC voltage, (b) grid current, (c) CHMI voltage, (d) Inverter current



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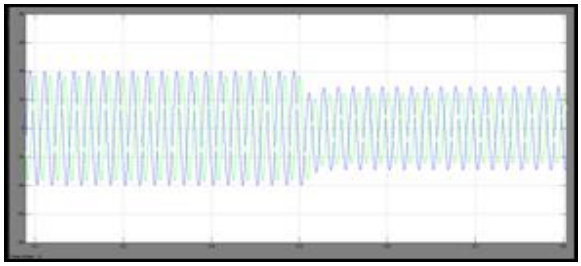

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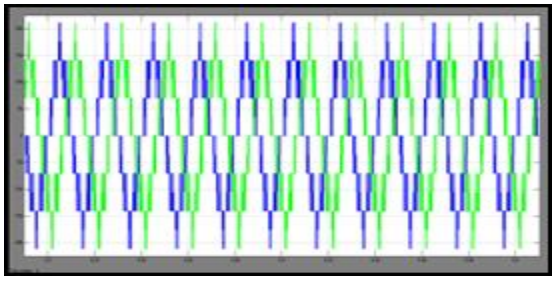

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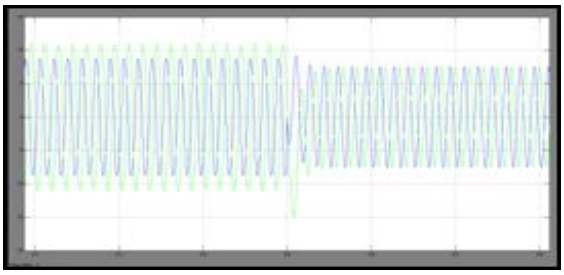

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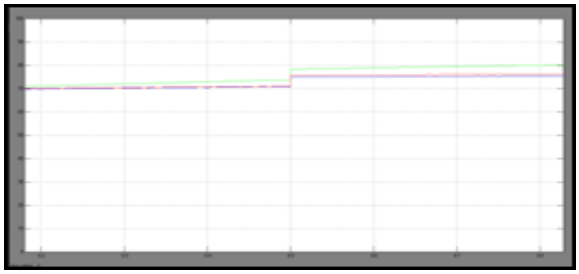

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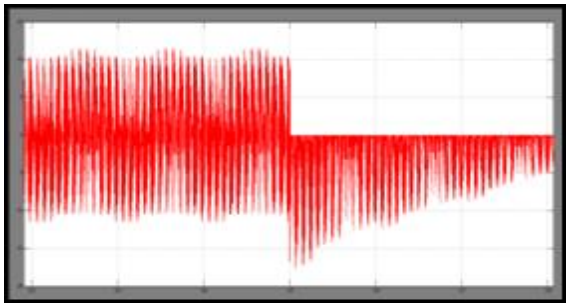
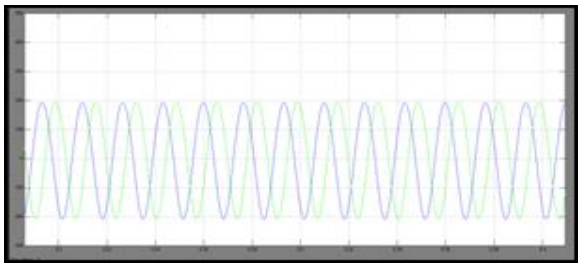


[f]

Fig: 13 fuzzy based Dynamic response of the SAPF CHMI to sudden changes in the load: fuzzy (a) PCC voltage, (b) grid current, (c) CHMI voltage, (d) Inverter current, (e) dc link voltage, (f) dc link current



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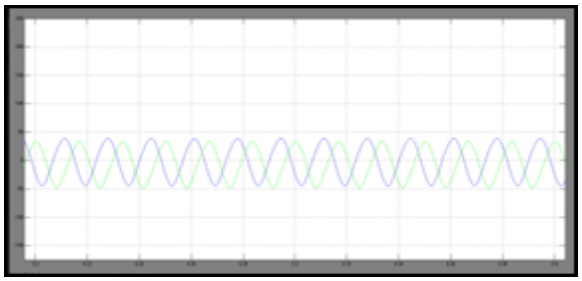

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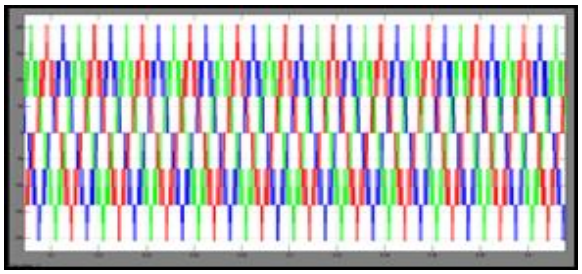

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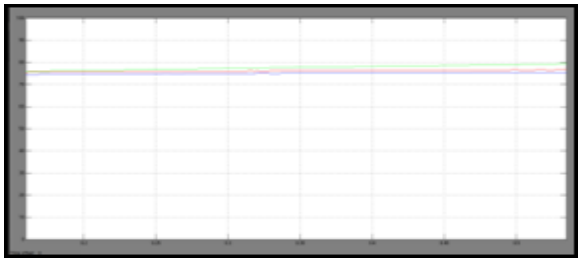

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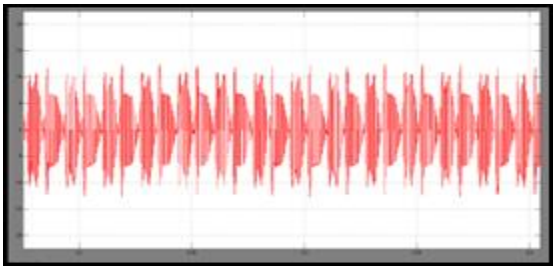
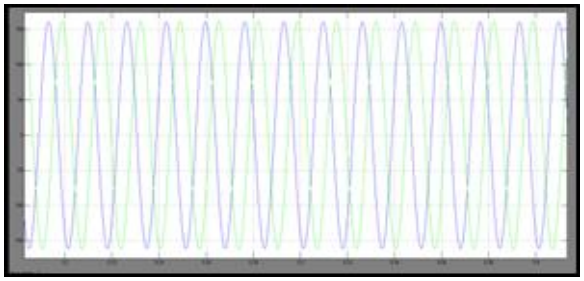


[e]

Fig: 14 fuzzy based Non fuzzy (a) PCC voltage, (b) grid current, (c) CHMI voltage, (d) Inverter current, (e) dc link voltage, (f) dc link current



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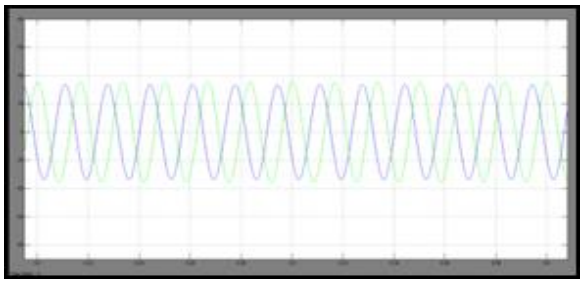

[b]

Fig: 15 fuzzy based Compensation of ina current under asymmetrical and sinusoidal voltage source fuzzy [a] PCC voltage, [b] grid current

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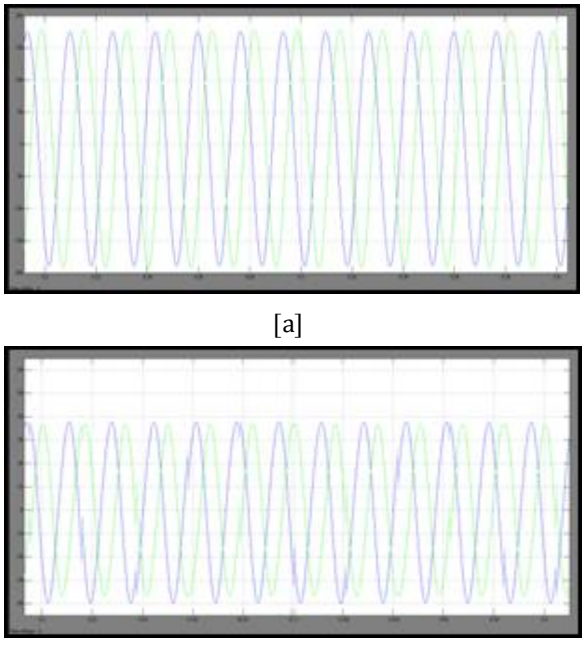

[a]

[b]

Fig: 16 fuzzy based Compensation of ina current under symmetrical and non – sinusoidal voltage source: fuzzy [a] PCC voltage, [b]grid current

THD Values:

MODE	WAVE FORM	THD values by using PI Controller	THD values by using Fuzzy Controller
Before implementing any compensation strategy	PCC voltage	0.81	0.29
	Grid current	1.19	0.78
Reactive Current Compensation	PCC voltage	0.54	0.10
	Grid current	1.15	0.21
Unbalanced Current Compensation	PCC voltage	1.6	0.96
	Grid current	1.21	0.60
Harmonic Current Compensation	PCC voltage	0.81	0.29
	Grid current	1.21	0.89
Dynamic Performance of the CHMI under a Load Switching Event	PCC voltage	0.85	0.32
	Grid current	7.09	2.55
Non-active Current Compensation	PCC voltage	7.86	3.99
	Grid current	6.67	5.92
Asymmetrical and Sinusoidal Voltage Source with Va	PCC voltage	1.02	0.05
	Grid current	1.15	0.25
Symmetrical and Non-sinusoidal Voltage Source	PCC voltage	7.93	4.09
	Grid current	5.45	4.73

VI. CONCLUSION

This article proposes the utilization of a fell staggered shunt converter as an adaptable power conditioner, meaning to particular remuneration of aggravating current segments separated utilizing the Conservative Power Theory. Utilizing staggered converters has a few benefits, e.g., the seclusion in the framework setup with expanded unwavering quality, likewise permitting the utilization of autonomous DC connect voltages. These highlights independent from anyone else as of now make this topology a perfect possibility for medium and high power applications. Likewise, the created control technique manages the yield current by following references given by CPT, without actualizing any reference outline change.

In addition, CPT-based pay methodologies take into account the particular remuneration of unsettling influences brought about by burdens (receptive current, asymmetry, unbalances or nonlinearities). This is significant with respect to the assignment of duties on account of savvy miniaturized scale matrices or present day control frameworks.

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